

### Signal Limiter for Power Amplifiers

#### Abstract

Power amplifiers, when driven out of their linear range of operation, sound particularly bad, and can produce damage to themselves or the transducers to which they are connected.

The design of traditional protection circuits is complicated by the various performance, cost, and sonic tradeoffs involved. There is certainly no one right answer to the limiter puzzle. The circuits presented here, however, are designed to maintain a high level of sonic integrity, while remaining cost-effective.

These circuits combine active limiting with a diode-based clipper to provide excellent driver protection while avoiding the sonic degradation of simpler designs. An innovative nonlinear capacitor circuit further improves the sonic performance of the limiter.

The design is based on the THAT 4301 Analog Engine™, and thus requires only a single IC, a couple of transistors and diodes, and a handful of passive components.

### Signal Limiter for Power Amplifiers

The simplest circuits used to prevent overload in power amplifiers usually employ diode clippers. These have the advantages of being both fast and inexpensive. They also sound quite unpleasant when the amplifier is overdriven for more than a few tens of milliseconds. As a result, users may avoid fully exploiting the amplifier's available headroom because they fear the sonic results of overload. In the worst case, an amplifier with otherwise admirable performance may gain a reputation for poor sound quality.

The significantly improved version shown here employs two stages of protection — a VCA-based limiter which quickly and automatically reduces the input signal level to just below the overload point, and a conventional diode clipper to handle any short duration excursions while the limiter stage reacts.

The circuits shown are built around the THAT 4301 Analog Engine™. The THAT 4301 provides a single-chip solution for a variety of analog signal processing applications. It includes a high quality Blackmer gain-cell VCA, an RMS-level detector, and three general purpose op amps, two of which are undedicated. The circuits shown are easily adaptable for use with separate THAT Corporation VCAs and RMS-level detectors where even higher performance is required.

#### Assumptions

We will approach the design of the circuit using an approximately real-world example using the following assumptions:

1. The power amplifier's decibel voltage gain is 32 dB, a common value;
2. The maximum average power that can be dissipated by the 8Ω load is 600W;
3. The maximum peak power that can be dissipated by the 8Ω load is 6kW.

With these assumptions, we make the following calculations:

1. The voltage gain of the power amplifier is  $A_v = 10^{\frac{32}{20}} \approx 40$
2. Assuming a sine wave output, the output voltage at maximum average power dissipation is  $V_{out_{max\ avg P}} = \sqrt{600W \times 8\Omega} = 70V_{RMS}$
3. The output at maximum peak power dissipation is:  $V_{in_{max\ peak P}} = \sqrt{6000W \times 8\Omega} = 220V_{RMS}$ .

Knowing these values, we can calculate the appropriate limiter and clipper output voltages as

$$V_{in_{max\ avg P}} = \frac{70V_{RMS}}{40} = 1.75V_{RMS}$$

$$\text{and } V_{in_{max\ peak P}} = \frac{220V_{RMS}}{40} = 5.5V_{RMS}$$

## Basic Feedback Limiter with Diode Clipper

The circuit shown in Figure 1 demonstrates the basic feedback limiter with adjustable clipper. The input signal is fed to the limiter circuitry at the node labeled "Input". The limiter's output is sent to the power amplifier from the point labeled "To Power Amp Input". In addition, the output from the power amplifier is fed back to the limiter circuit by way of the node marked "From Power Amp Output".

Under normal operation, the input signal is below the limiter's threshold and so the VCA is at unity gain, its lowest distortion region.

For peak output levels of short duration which exceed the predetermined clip level, the clipper circuit "hard limits" the output to this level, performing very much like the (adjustable) diode clipper that it is. If

the output level remains above threshold for long, the signal's rms value will exceed the limiter's average power threshold, causing the limiter to quickly reduce the level of signal being fed to the amplifier. In this way, inaudible (but potentially damaging) peaks of short duration will be clipped, while longer duration peaks will be handled by the limiter, and little audible impairment should occur.

### The Clipper

Figure 2 shows the clipper circuit used in this design. A trans-impedance amplifier, OA3, converts the output current from the VCA to a voltage which drives the actual clipper circuitry. When OA3's output voltage exceeds the threshold set by VR1, the transistor pair Q1 and Q2 combine to bypass R2 and clip the output to a fixed level.

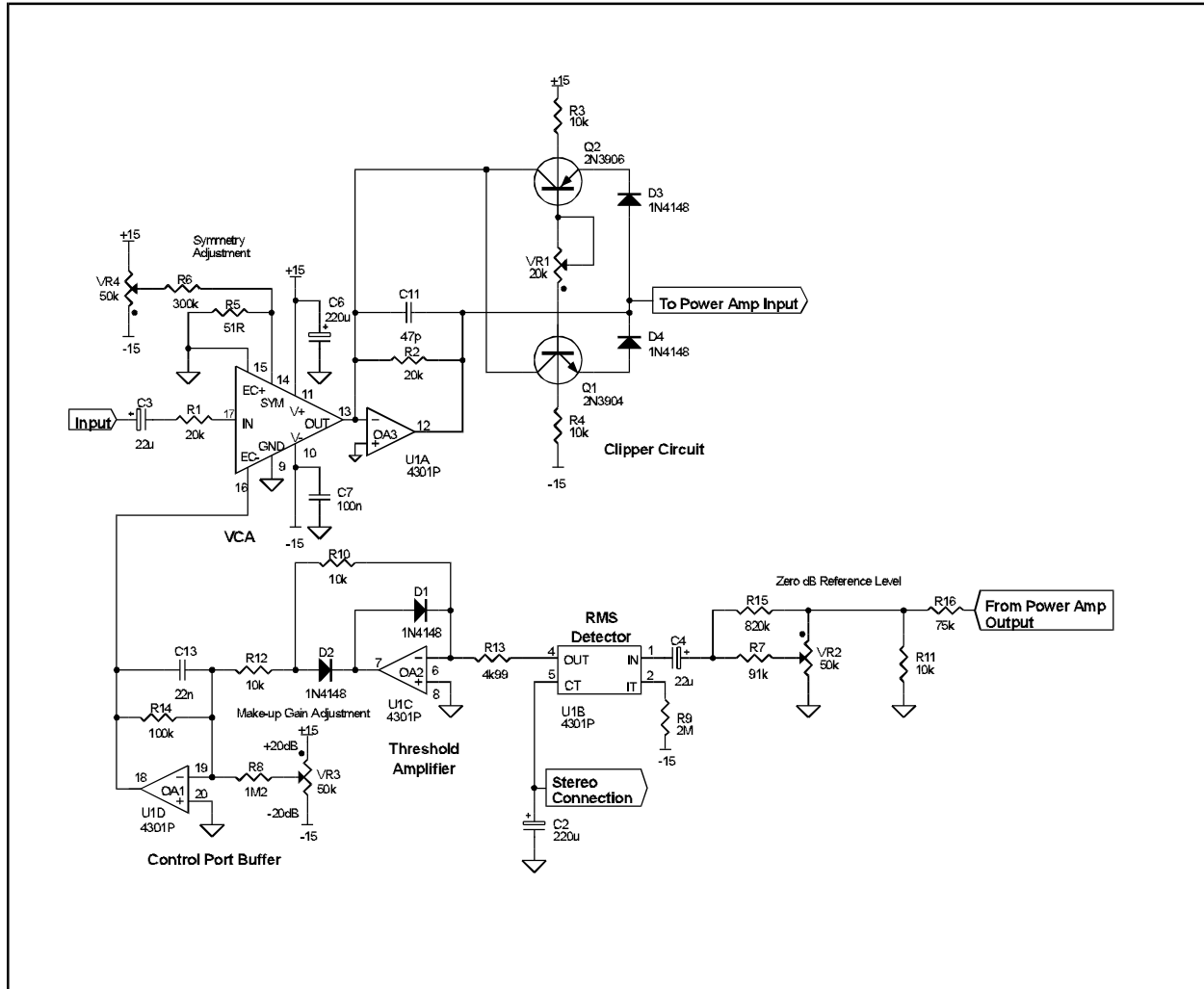


Figure 1. Schematic of basic signal limiter

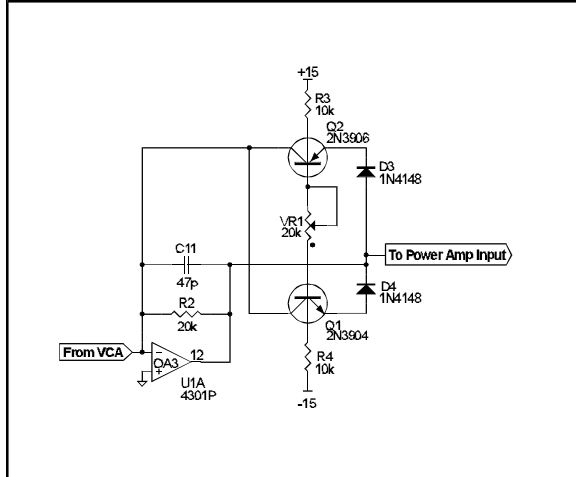


Figure 2. Detail of clipper circuit

Using our design example, the peak allowable power is specified as  $200V_{RMS}$ , and since we are ultimately clipping the signal to a square wave, this is equivalent to  $220V_{peak}$ . Given the power amplifier's gain of 40, the limiter must clip at  $5.5V_{peak}$ .

The two 1N4148 diodes prevent base-emitter breakdown in Q1 and Q2. The addition of these diodes means that the clipping voltage will be two diode drops (approximately 1.2V) greater than the voltage at the bases of Q1 and Q2. VR1 adjusts the voltage at the base of Q1 between 0 and -7.5V, and at the base of Q2 between 0 and +7.5V. Since we want the limiter to clip at 5.5V, VR1 should be adjusted to provide -4.3V and 4.3V at the bases of Q1 and Q2, respectively.

**The Limiter**

To form the limiter block, the VCA in Figure 1 is configured as a high-compression-ratio feedback compressor. Under normal operation, the amplifier output is below the compressor's threshold voltage, the VCA's  $E_c$  control port is kept at zero volts, resulting in no compression or limiting action. Above the threshold level, the threshold amplifier conducts and closes the feedback loop from the RMS level-detector to the VCA, resulting in the desired limiter function.

Figure 3 shows a simplified diagram of a feedback (FB) compressor. By inspection,

$$V_{out\ dB} = V_{in\ dB} + G_{dB}$$

and

$$G_{dB} = -A \times V_{enc\ dB}, \text{ where}$$

1.  $V_{in\ dB}$  is the input level in decibels and  $V_{out\ dB}$  is the output level in decibels,
2.  $G_{dB}$  is the VCA gain in decibels, and
3.  $A$  is the gain between the detector and the control port of the VCA.

The minus sign in the side-chain gain equation comes from the fact that this is a compressor circuit, and the gain of the VCA moves in the opposite direction of output signal amplitude.

Combining these equations yields

$$V_{out\ dB} = V_{in\ dB} - A \times V_{out\ dB}$$

which can be rearranged to form

$$\frac{V_{in\ dB}}{V_{out\ dB}} = 1 + A.$$

This is the compression ratio of the compressor. To get the compressor to act as a limiter, we need to set the compression value to a high value. A suitable and convenient value is 21, and we can calculate the gain required to achieve this compression ratio as

$$A = \frac{V_{in\ dB}}{V_{out\ dB}} - 1 = 21 - 1 = 20.$$

A side-chain gain of 20 will, therefore, yield a compression ratio of 21, resulting in the expected limiter behavior.

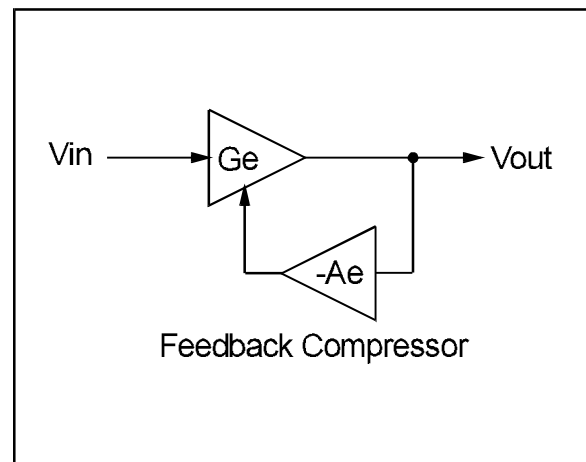


Figure 3. General feedback compressor topology

### The RMS Level-Detector

THAT Corporation's RMS level-detectors generate an output voltage that is proportional to the signal power in decibels. A user-programmable "reference level" determines the signal level for zero volts output from the detector. The detector output will then swing positive (for input signal levels above the reference level) or negative (for signals below reference) at a constant 6mV/dB.

To calculate the true-rms value of an ac input signal, THAT's RMS level-detectors first full-wave rectify, then log the signal. The logged signal is then doubled, which effectively squares the signal since the operation is carried out in the log domain. The subsequent square root operation is actually performed implicitly at the exponential input of the VCA.

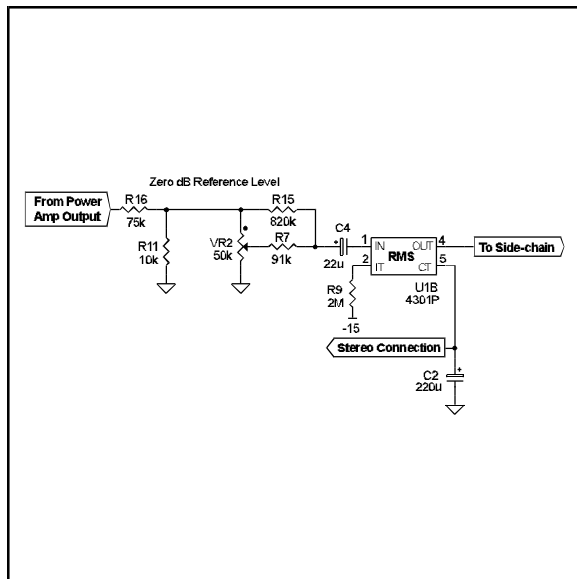


Figure 4. Detail of RMS detector circuitry

The "mean" operation is carried out by filtering the rectified and logged signal, and it is this log-domain filter that sets the time constants (attack and release times) for the limiter. Referring to Figure 4, the log-domain filter consists of an internal diode biased by a fixed DC current ( $I_T$ ), along with external components R9, which establishes  $I_T$ , and C2, the timing capacitor itself. The time constant of the filter is calculated from:

$$\tau = C_2 \times \frac{V_T}{I_C}$$

and therefore

$$C_2 = \frac{1}{2 \times \pi \times f_c \times \frac{V_T}{I_C}}$$

A compromise is involved in setting the filter time constants, because the filter also must smooth the rectified and logged input signal. Without the smoothing operation, the 2nd harmonic generated by the rectification process result in high levels of 3rd harmonic distortion in the output of the VCA. With this in mind, the filter time constants must balance the need for low distortion with continuous signals against the need for fast operation in the presence of transients.

From long experience, a cutoff frequency of approximately 5Hz has been found to be an effective compromise. This frequency is well below the audio band and is sufficient to keep distortion low. The recommended value for  $I_T$  (the timing current) is 7.5 $\mu$ A, resulting in a timing capacitor of approximately 10 $\mu$ F.

A better solution to the distortion vs. speed issue is presented later in this paper as *Extra Credit: The Nonlinear Capacitor*.

The above calculations assume a stand-alone RMS level-detector. When the detector is placed in a feedback compressor topology, the effective time constant that results is calculated by taking the level detector's stand-alone time constant and dividing it by the compression ratio. Therefore, if we plan to operate with a compression ratio of, say, 20:1, we will need to increase the timing capacitor by a factor of 20. So, for our design the timing capacitor, C2, becomes 220uF, the nearest standard value.

The timing current is set by R9, and is calculated as

$$R_T = \frac{-V_{SS}}{I_T} = \frac{15V}{7.5\mu A} = 2M\Omega.$$

Knowing this, we can calculate the "zero dB reference current" for the RMS level-detector (recall that this is the input current which result in zero volts output from the detector. This is also the value that will produce unity gain through the VCA):

$$I_{ref} = 1.13 \times I_T = 8.5\mu A.$$

As previously stated, this circuit is specifically designed to limit at 70V<sub>RMS</sub>. However, for the sake of

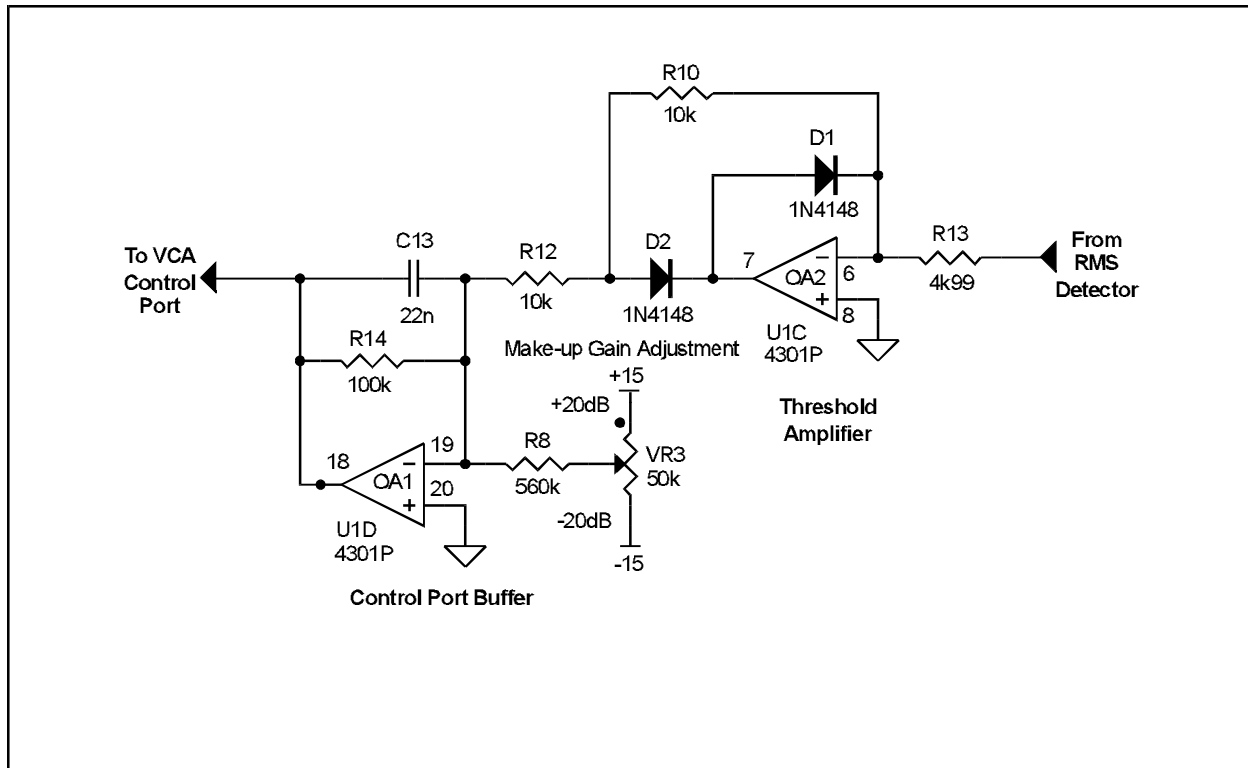


Figure 5. Detail of side-chain circuitry

flexibility, we are going to provide a trim to accommodate a range of  $7\text{-}70V_{\text{RMS}}$  by adding the resistive pad composed of R16, R11, and VR2. This results in an approximately 10:1 divider.

With this pad in place, a  $70V_{\text{RMS}}$  input is reduced to  $7V_{\text{RMS}}$  at the top of the potentiometer. Now the input to the RMS level-detector can be treated as a virtual ground. Knowing this, along with the detector's reference level, we can calculate the largest value of input resistor required as,

$$R_{\text{RMSin}} = \frac{7V_{\text{RMS}}}{8.5\mu\text{A}} = 820\text{k}\Omega.$$

This is the value that will be seen by the detector when the wiper of VR2 is at the bottom of its range.

At the other extreme, we desire the limiter to respond at a power amplifier output of  $7V_{\text{RMS}}$ . At this level, the 10:1 pad will result in  $0.7V_{\text{RMS}}$  at the top of VR2. The resistor value required to generate the detector's reference level is

$$R_{\text{RMSin}} = \frac{0.7V_{\text{RMS}}}{8.5\mu\text{A}} = 82\text{k}\Omega$$

By choosing a value of  $91\text{k}\Omega$  for R7, we get  $81\text{k}\Omega$  as the parallel combination of R15 and R7 when VR2 is at the top of its range.

### The Side-chain

The circuit in Figure 5 shows an isolated view of the side-chain of Figure 1. When the signal is above the limiter threshold voltage, the gain for the threshold amplifier is,

$$A_{\text{threshold}} = \frac{-R10}{R13} = \frac{-10\text{k}\Omega}{4.99\text{k}\Omega} = -2.$$

The gain of the control port buffer is,

$$A_{\text{buffer}} = \frac{-R14}{R12} = \frac{-100\text{k}\Omega}{10\text{k}\Omega} = -10$$

for a net gain of 20.

To make the circuit more versatile, an optional "make-up gain" circuit comprised of R8 and VR3 has been added to allow for convenient manual gain adjustment of the limiter circuit over a range of  $\pm 20\text{dB}$ . To calculate the sensitivity of the make-up gain cir-

cuit, we first compute the current sensitivity at the inverting input of OA1,

$$\frac{I}{dB} = \frac{6.5 \frac{mV}{dB}}{R12} = \frac{13 \frac{mV}{dB}}{10k\Omega} = 1.3 \frac{\mu A}{dB}$$

Since the maximum voltage across R8 is  $\pm 15V$ , and we want the resulting current to cause a  $\pm 20dB$  swing,

$$R8 = \frac{15V}{20 \times 1.3 \frac{\mu A}{dB}} = 576k\Omega.$$

560k $\Omega$  is the closes 5% value to the calculated value.

### Other Issues

The VCA in the THAT 4301, like all of the THAT Corporation's Blackmer gain-cell VCAs, operates in Class AB mode. Due to minor differences between the transistors in the gain cell, there is often a slight asymmetry between the gain of upper and lower halves of the output waveforms. The result of this asymmetry is a potential maximum THD+N of 0.7% at unity gain.

If this maximum THD+N is acceptable in a given application, no external distortion trim (R6 and VR4 in Figure 1) is required. This might be the case, for

example, where the limiter is feeding a subwoofer amplifier or other low-fidelity application.

With the distortion trim, THD+N can be reduced to maximum 0.007% (unity gain with 0dBV input at 1kHz).

An important application consideration concerns the bypassing and layout of the THAT 4301. As was mentioned in the section on the RMS level-detector, the timing capacitor is part of a log filter composed of the capacitor and a diode internal to the IC. During transients, the diode will conduct only during short periods, and this can result in high peak currents. In order to prevent these currents from injecting unwanted signals elsewhere in the circuit, a charging current path directly from  $V_{CC}$  is usually required.

To accomplish this, C6 should be placed so that its grounded side is close to the grounded side of C2, and these two devices should connect to each other before connecting to system ground.

### Closing Thoughts

Although speaker protection can be had with lower-cost amplifier clipping circuits, peaks of long duration may still result in speaker damage. As well, the sound of low-cost clippers may keep users from

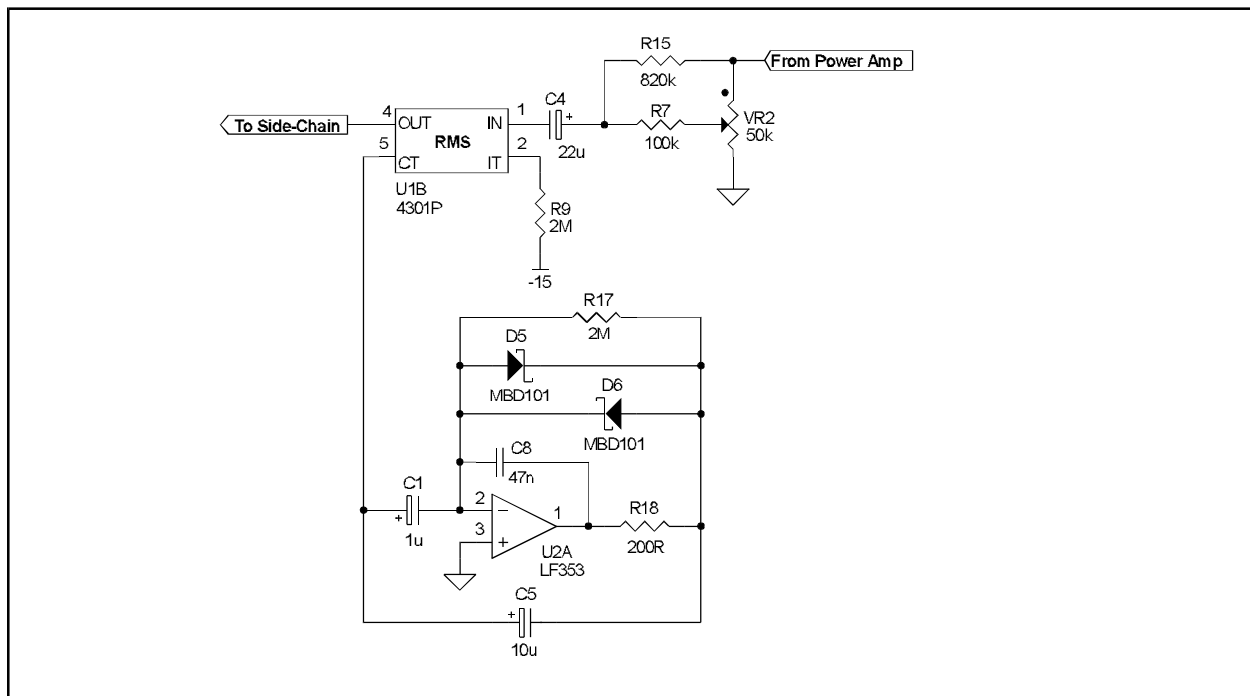


Figure 6. RMS detector with nonlinear capacitor circuit

using the maximum headroom available from an amplifier.

The high-fidelity limiter described in this application note keeps an amplifier sounding good even when its input is overdriven. The result is a cleaner, more powerful impression, and better protection for the speaker system.

## Extra Credit: The Nonlinear Capacitor

We mentioned earlier that RMS level-detectors exhibit low-frequency 2nd harmonic ripple (the result of their finite averaging time) which results in a 3rd harmonic component from the VCA. We nearly eliminated this component by way of the log filter capacitor, C2. However, while increasing the value of this capacitor provides good distortion performance, it also results in slower response time than may be desired in some applications.

In order to keep distortion low and provide rapid response to transient signals, a “nonlinear capacitor” (NLC) circuit can be incorporated in the design. This circuit effectively changes the timing capacitor value based on the characteristics of the incoming signal.

In the NLC circuit, the RMS level-detector is configured as a typical detector, but the timing capacitor is replaced with C1 (see Figure 6), which is connected to the virtual ground of op amp U2A. The gain of this stage is set by the ratio of C1 and C8.

Dynamically, C1 and C5 are in parallel. Under conditions where the op amp’s output is not limited by D5 and D6 (“slow mode”), C5 is effectively multiplied by one minus the closed-loop gain of the U2A, the result of the well-known Miller Effect. When D5 and D6 limit the output of the op amp, C5 (with no Miller Effect multiplication factor) is simply in parallel with C1 (“fast mode”).

The simplified transfer functions for this circuit are:

$$\text{For Steady-State Inputs: } C_{Time} = C1 + C5 \times \left(1 + \frac{C1}{C8}\right)$$

$$\text{For Transient Inputs: } C_{Time} = C1 + C5.$$

Here are some important design equations and a few tips on fine-tuning the values in the NLC circuit:

1. The value of R17, the resistor which provides a return path for the op amp’s bias current, is chosen to produce a minimal DC offset as a result of the bias

current. If your diodes are leaky, you may be able to use a much larger value of R17.

2. The value of C8 is chosen so that  $f_c$  resulting from C8 and R17 is below the audio range,

$$f_c = \frac{1}{2\pi \times R17 \times C8} = 1.6\text{Hz.}$$

3. Let us first look at It may be shown that, when log-based RMS level-detectors are connected to exponentially-controlled VCAs, the ratio of the ripple-induced 3rd harmonic to fundamental for a given  $\tau$  at a given frequency  $\omega$  is,

$$\frac{I_{3rd}}{I_{1st}} = \frac{1}{4\sqrt{1 + (2\omega)^2 \tau^2}}.$$

This may be rearranged to give,

$$\tau^2 = \frac{\left(\frac{I_{1st}}{4 \times I_{3rd}}\right)^2 - 1}{(4\pi f)^2}.$$

Presumably, one intends to design a low distortion circuit and, therefore, we may assume that,

$$\frac{I_{1st}}{I_{3rd}} \gg 1.$$

Consequently,

$$\tau^2 \approx \frac{\left(\frac{I_{1st}}{4 \times I_{3rd}}\right)^2}{(4\pi f)^2}$$

And we may then state that,

$$\tau \approx \frac{\left(\frac{I_{1st}}{4 \times I_{3rd}}\right)}{(4\pi f)} = \frac{I_{1st}}{16\pi f \times I_{3rd}}.$$

Assume that we are willing to accept 1% THD+N at 50Hz. We can then calculate (for slow mode operation),

$$\tau_{SLOW} \approx \frac{I_{1st}}{16\pi f \times I_{3rd}} = \frac{1}{16\pi f} \times \frac{I_{1st}}{I_{3rd}}$$

or

$$\tau_{SLOW} \approx \frac{1}{16\pi \times 50\text{Hz}} \times 100 = 0.04\text{s}.$$

A relatively complex analysis that is beyond the scope of this paper will show that the average ripple voltage at a given  $\tau$  and frequency is,

$$V_{Ravg} = \frac{V_T}{2\sqrt{2} \times \omega\tau} = \frac{V_T}{4\pi\sqrt{2} \times ft}.$$

At room temperature,  $V_T = 26\text{mV}$ , and from our design requirement, the frequency of interest is 50Hz. Therefore,

$$V_{Ravg} = \frac{0.026\text{V}}{4\pi\sqrt{2} \times 50\text{Hz} \times 0.04}, \text{ or}$$

$$V_{Ravg} = 731\mu\text{V} = 1.03\text{mV}_{\text{peak}}.$$

We can convert this to decibels by dividing the result by the THAT 4301's control voltage constant (6.5mV per dB),

$$V_{Ravg\text{dB}} = \frac{1.03\text{mV}}{0.0065 \frac{\text{V}}{\text{dB}}} = 0.16\text{dB}.$$

4. Let us assume that we want the NLC's fast mode to be 20 times faster than the slow mode. We can use the equation,

$$C_{Slow} = C.R. \times \tau_{SLOW} \frac{I_T}{V_T} \approx 220\mu\text{F}$$

(where C.R. = the compression ratio)

to determine the required effective timing capacitance in slow mode. The fast mode capacitance would then be,

$$C_{Fast} = \frac{C_{Slow}}{20} = 11\mu\text{F}.$$

The slow mode capacitance is calculated as,

$$C_{Slow} = C1 + C5(1 + \frac{C1}{C8})$$

whereas the fast mode capacitance is simply C1 in parallel with C5, or

$$C_{Fast} = C1 + C5.$$

Since we already know our desired fast capacitance,

$$C1 = 11\mu\text{F} - C5.$$

5. The required gain is determined by calculating how many decibels will correspond to a single diode drop. Green LEDs have a forward drop of approximately 2.2V, while red LEDs have a forward drop closer to 1.6V. Anti-paralleled silicon diodes have a forward drop of about 0.65V, and anti-paralleled Schottky and germanium diodes have a forward drop of approximately 0.4V (all depending, of course, on the current through the diode).

We choose to allow 3dB of change at the detector output before the diodes turn on and switch to fast mode. This provides ample margin above the 0.16dB calculated in section 3 above, thus preventing 50Hz sine wave signals from activating fast mode.

If we use Schottky diodes, and allow for the 3dB swing before diode turn-on,

$$A_v = \frac{0.4\text{V}}{3\text{dB} \times 6.5 \frac{\text{mV}}{\text{dB}}} \approx 20.5$$

which sets the ratio of the gain-setting capacitors,

$$A_v = \frac{C1}{C8}.$$

Note that if an even larger band is needed, one may use the transistor arrangement shown in Figure 2 in place of diodes in this circuit.

6. Combining some of the equations in 4 and 5 above, we may state that,

$$C1 + C5 \times 21.5 = 220\mu\text{F}$$

and

$$C1 + C5 = 11\mu\text{F}.$$

It follows that,

$$11\mu\text{F} - C5 + C5 \times 21.5 = 220\mu\text{F},$$

and then

$$C5 = \frac{220\mu\text{F} - 11\mu\text{F}}{20.5} = 10.2\mu\text{F}.$$

We can now determine that

$$C1 = 11\mu\text{F} - 10.2\mu\text{F} \approx 1\mu\text{F},$$

and finally

$$C8 = \frac{C1}{20.5} = 47\text{nF}.$$

This circuit can be used to replace C6 in Figure 1. By doing so, the basic limiter circuit becomes much more flexible, eliminating the need to trade fast attack times for distortion performance.

## **Notes**